Silicon integrated electrical micro-lens for CMOS SPADs based on avalanche propagation phenomenon

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***Abstract*– The design and fabrication of integrated micro-lenses for CMOS single-photon avalanche diodes (SPADs) is presented in this paper. The micro-lens exploits the avalanche propagation phenomenon occurring in abrupt single-sided junctions and is achieved by carful design of the SPAD in a standard CMOS process. In contrast to an optical micro-lens, the proposed technique is more robust to manufacturing tolerances and can scale in principle to large arrays, providing a better concentration factor and concentration uniformity. Measurement results show a photon detection probability (PDP) as high as 64.85 % at 600 nm when the SPAD is biased at 2 V of excess bias. The micro-lens configuration is compatible with backside illumination and the use of integrated devices on guard rings, thereby enabling the high density pixels and extremely high fill factors.**

I. Introduction

Single-photon avalanche diodes (SPADs) are p-n junctions biased above breakdown, in so-called Geiger mode. In this mode of operation the high electric field present in the depletion region exceeds the value necessary to support multiplication of photoelectrons or holes by impact ionization. In the recent past, the evolution from single SPADs to SPAD arrays has enabled the emergence of imagers for photon-starved biomedical and microscopy applications. However, the requirement to maximize photon detection efficiency (PDE) has created the need for increased fill factor.

In a conventional SPAD design, as presented in [1], guard rings, contacts, and readout circuitry limit the fill factor. To recover the loss of incident photons in the guard region, micro-lenses or prisms have been used, so as to concentrate light from insensitive to sensitive areas of the pixel, known as active area. However, due to manufacturing tolerances, concentration non-uniformity, and reproducibility issues, robust solutions have not been achieved for arrays larger than 1 kpixel [2]. Alternatively, backside-illuminated (BSI) designs [3] have been proposed for avalanche photodiodes (APDs) and SPADs, however, it is not clear at the time of the writing of this paper, whether BSI will be a viable option for SPADs in the near future.

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In this paper, we address the challenges associated with optical microlenses, with a concentration technique that is not optical but electrical in nature. The technique is based on lateral avalanche propagation (LAP) [4], [5], [6]; its purpose is to enable photocarriers generated in the periphery, usually subject to recombination, to trigger Geiger pulses.

In contrast to drift, that moves photocarriers along the field lines without multiplication, LAP acts along the junction perpendicularly to the electric field (parallel to the surface), thus enabling radial movement of carriers towards the center of the structure. In the past, the use of LAP has been limited to the active area only, for position-sensitive SPADs [7] and fix-position noise reduction [8]. In this paper, we expand the use of LAP far beyond the active area for acquiring photocarriers from below the guard ring regions and from other deep-well regions hosting CMOS circuits.

II. Design and Implementation

To enable the creation of an avalanche under the guard ring region, the SPAD is designed to operate near the guard ring region's breakdown voltage, i.e. the breakdown voltage of the guard ring is 2 V higher than that of the multiplication region. Further, to achieve identical spectral response everywhere, the guard ring region and multiplication regions were designed to have virtually the same depth.

The proposed concept is shown in Fig. 1. The figure depicts the cross-section of the device and the avalanche propagation pattern below the guard ring.

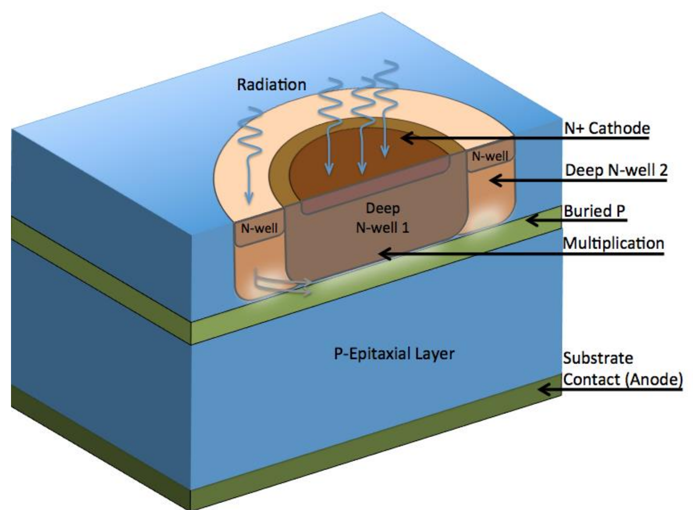


Fig. 1: Designed SPAD junction in CMOS process along with its guard region design.

The device was carefully designed using the appropriate semiconductor layers and junctions to achieve adequate electric field profiles. To validate the electric field profiles for the designed device, extensive simulations were performed using MEDICI. In the guard ring region, an electric field of $4x10^5$ V/cm was designed, to be close but not equal to the critical field that supports impact ionization in silicon. This high electric field is required to enhance the avalanche triggering probability in Geiger mode, thus leading to the acquisition of photons from guard ring regions. Fig. 2 shows the amplitude and direction of the electric field in the proposed device, as a result of simulations using MEDICI.

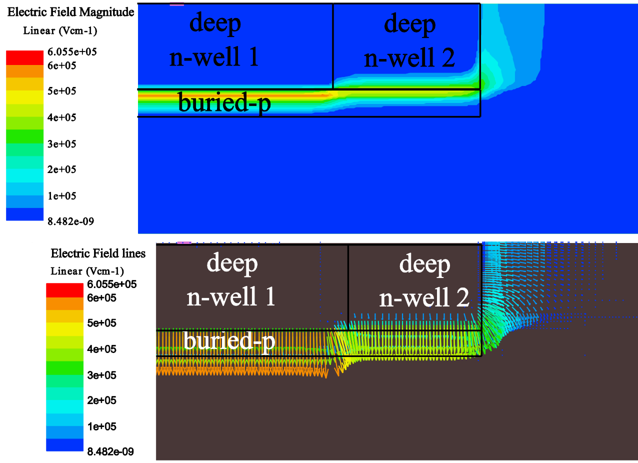


Fig. 2: Device electric field magnitude and direction simulated using MEDICI at the active regions breakdown voltage.

To validate the proposed technique, two devices with two different guard ring (deep n-well 2) widths, 4µm (device 1) and 12µm (device 2), were designed and fabricated for an active area (deep n-well 1) with a diameter of 12µm. A photomicrograph of the fabricated device (device 1) is shown in Fig. 3.

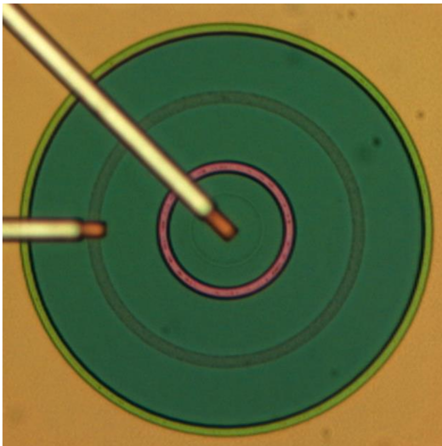


Fig. 3: Device Micrograph. In this device the guard ring width is 4µm; the active area has a diameter of 12µm.

III. Experimental results

A. I-V Measurements

Measurements performed on device 1 and 2 have shown a sharp reverse I-V breakdown characteristics at 26.4 V and 26.2 V respectively, at room temperature. Fig. 4 shows the I-V characteristics for both devices at room temperature.

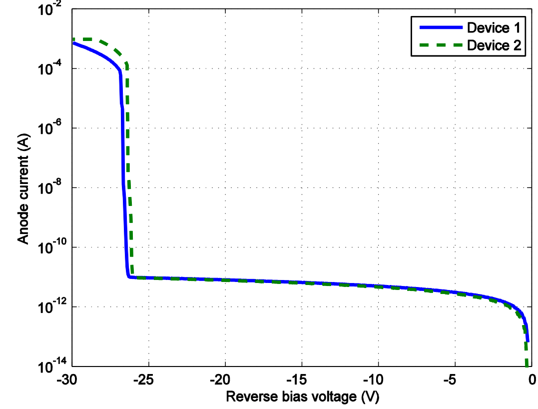


Fig. 4: I-V measurements performed on two test structures of 4µm (device 1) and 12µm (device 2) guard width for a 12µm active diameter.

B. Light emission test

Further, to study the spatial distribution of high electric field region, light emission tests (LETs) [9] were performed at various bias conditions. LET results (Fig. 5) have confirmed that at the device's breakdown voltage, a high electric field region resides only in the designed active area (beneath deep n-well 1). At little above 2V of excess bias, as expected, the high electric field region spreads to the guard ring area (beneath deep n-well 2).

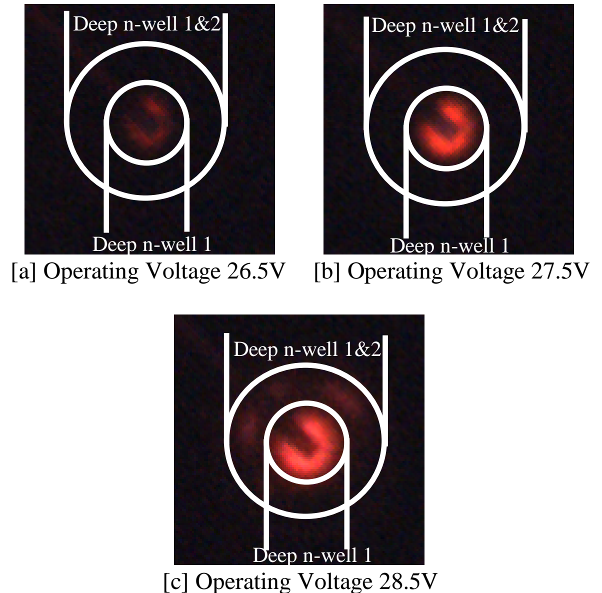


Fig. 5: Light emission test performed at various bias voltages for device 1. In (a) the operating voltage (breakdown + excess bias) is 26.5V, in (b) 27.5V, and in (c) 28.5V. All measurements were conducted at room temperature.

C. *Dark count rate (DCR)*

For the DCR measurements the devices were operated in Geiger mode using external quenching and recharge circuitry. The designed circuitry provided fixed quench and recharge time thereby eliminating any impact on dead time due to parasitic capacitances of device 1 and 2. The circuitry is shown in Fig. 6. A fast comparator detects an avalanche event and a feedback loop controls the recharge of the SPAD providing enough current to recharge the parasitic capacitance present at the cathode of the SPAD. The anode is placed at a negative voltage corresponding to the breakdown voltage, while the excess bias voltage is applied on the other pin of the quenching resistor.

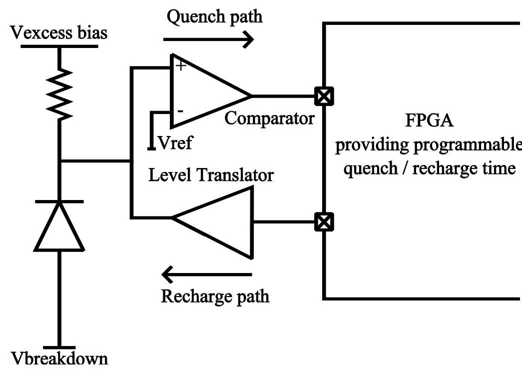


Fig. 6: Experimental setup: external active quenching/recharge circuitry mitigates the possible impact of device capacitance on measurements.

Both designs in 4 different dies have shown that device 2 (12 µm guard ring) becomes saturated at 0.25V of excess bias, due to dark noise. However, device 1 (4 µm guard ring) was found to be operational until 2.5V of excess bias, as shown in Fig. 7.

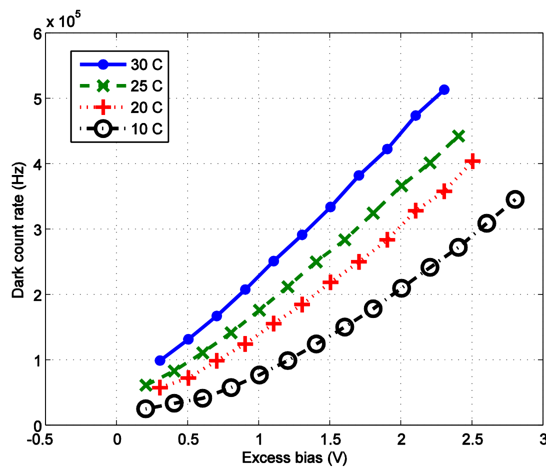


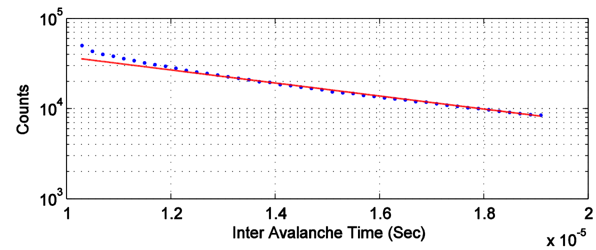
Fig. 7: DCR vs. excess bias at various temperatures for device 1.

It is to be noted that device 1 and 2 are designed for the same active area (deep n-well 1 size), with the only difference being the size of the two guard rings. The saturation effects observed for device 2, suggest that additional noise leading to saturation is generated in the guard ring region. Though, in the presented scenario, the guard ring region generated noise is collected, this observation confirms the existence of LAP.

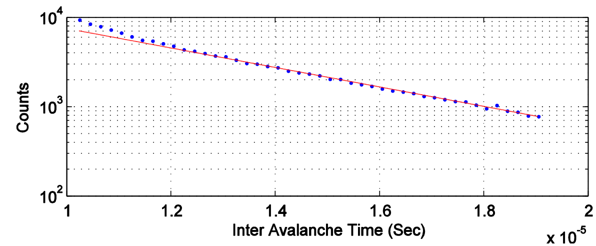
Further, the DCR measurements performed on device 1 at various temperatures and at various excess bias conditions show a stronger dependence of DCR on excess bias, than to temperature. This observation suggests that the major contribution to DCR originates due to tunneling. Hence, extensive work is underway in reducing the tunneling generated noise with a comprehensive doping profile optimization study.

D. *Afterpulsing probability*

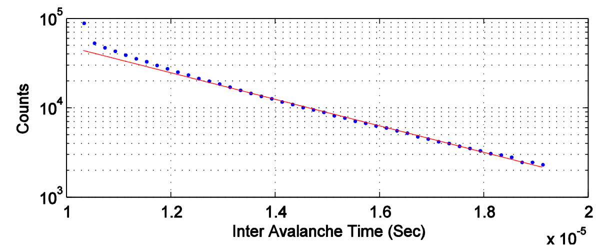
The afterpulsing probability measurements were carried out as described in [10]. In these measurements device 1 was used along with the external circuitry tuned to provide 10µs of quench time. The experimental results at various excess biases are presented in Fig. 8.



[a] Afterpulsing probability at 1.0V excess bias voltage: 7.2%



[b] Afterpulsing probability at 1.5V excess bias voltage: 8.1%



[c] Afterpulsing probability at 2.0V excess bias voltage: 14.3%

Fig. 8: Afterpulsing probability measurements. In (a) the excess bias is 1.0V, in (b) 1.5V, and in (c) 2.0V. All measurements were conducted at room temperature.

Although the measured afterpulsing is 7% or higher, it is to be noted that in the current setup the quench and the recharge circuitries are external, with a high parasitic capacitance due to bond pads and wires. We expect that the integration of external circuitry on to silicon can reduce the afterpulsing probability.

E. Photon detection probability (PDP)

The PDP measurements performed on device 1 are reported in Fig. 9. The presented results were obtained considering 12µm (deep n-well 1 size) for active diameter and with afterpulsing compensation. As expected, the PDP has increased drastically from 35.24% to 64.85% at a wavelength of 600 nm, when biased at 1.5V (bellow guard ring region breakdown) and at 2.0 V (at guard ring region breakdown) respectively. The measured result confirms the fact that, when biased at 2.0 V of excess bias, the region beneath the guard ring is activated leading to photon sensitivity. As expected, the PDP increase observed here is much greater than the normal increase due to excess bias.

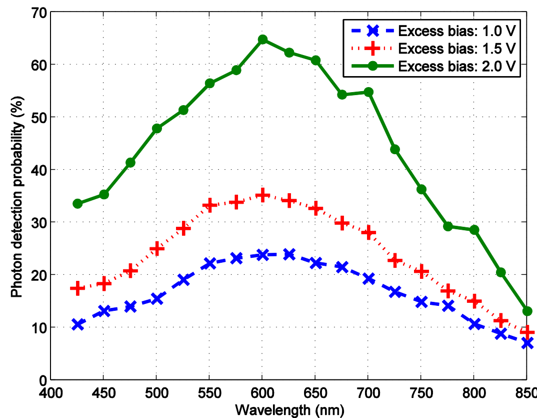


Fig. 9: Measurement results on photon detection probability for device 1 at various excess bias.

IV. Evolution

In this paper we have demonstrated that the space occupied by the guard ring can be recovered completely using the concept of electrical micro-lens. However, the guard ring can also be used to host circuitry, thereby enabling a virtual 100% fill factor, even in front-illumination configurations.

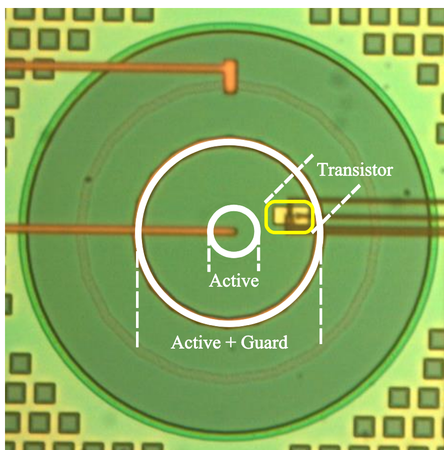


Fig. 10: Micrograph of the design with a quenching transistor in the guard ring region.

Triple-well processes enable the integration of both polarities, thus a fully insulated CMOS circuit can be implemented on it. Fig. 10 shows a test circuitry placed on the guard ring for the same devices presented in the paper. All the layers used in this device, except for the metals, have a low degree of opaqueness, thus making them ideal for front-illuminated configurations, while being obviously fully compatible with BSI configurations.

The transistors seen in the figure can be both PMOS and NMOS. Since the circuitry will be digital, small optically induced currents and transconduction variations will have negligible impact on the overall functionality.

V. Conclusion

The proposed technique to acquire photons from the guard ring region using the avalanche propagation phenomenon was successfully implemented and tested. Although the proposed technique enables to acquire photons outside active area, it is also sensitive to noise generated in the guard ring region. Currently we are considering various options to improve signal-to-noise ratio. The proposed technique is also suitable to be extended to other inactive areas in the pixel for further improvement of fill factor in multi-pixel image sensors.

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